REMARKS

Claims 1, 10, and 19 are amended, no claims are canceled, claim 96 is added; as a result, claims 1-23 and 85-96 are now pending in this application.

Applicant herein amends claims 1, 10 and 19 to clarify same. Specifically, claim 19 is amended to include the article "the" before "first metal layer." Claims 1 and 10 clarify the graded barrier layer.

§102 / 103 Rejection of the Claims

Claims 1, 3, 4, and 9 were rejected under 35 U.S.C. § 102(b) for anticipation by, or in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Endo (U.S. 5,619,051). Withdrawal of the rejection is respectfully requested.

Applicant respectfully submits that Endo does not teach all the elements recited in claim 1. The Office Action admits that a difference exists between Endo and the current subject matter in that Endo does not explicitly and positively disclose the limitation "asymmetrical" for the low tunnel barrier intergate insulator. The Office Action also admits another difference between Endo and the claimed subject matter, in that the low tunnel barrier intergate insulator is formed by a CVD (deposition) process rather than by multiple ALD deposition process recited in claim 1.

The Office Action states that "as for the limitation "asymmetrical", the reference discloses that, as noted above, proportions of the two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate to the top plane." (OA page 3, paragraph 3). Applicant has amended claim 1 to recite "wherein the control gate is separated from the floating gate by a *graded* asymmetrical low tunnel barrier intergate insulator formed by multiple atomic layer deposition (ALD)."

As the Office Action admits, Endo discloses a step-wise configuration of the low tunnel barrier intergate insulator. Endo discloses only a step-wise configuration because Endo uses a CVD (deposition) process to form the low tunnel barrier intergate insulator. A CVD process is believed to be incapable of forming what is commonly known in the art as a monolayer. A

monolayer is a very thin film. Because a CVD process is incapable of producing films with a thickness as small as a monolayer, it follows that a CVD process is also incapable of producing a graded low tunnel barrier intergate insulator. A CVD process is only capable of producing a larger thickness. Therefore, a CVD process is only capable of producing layers of low tunnel barrier intergate insulator in discrete increments, or "stepwise".

On the other hand, an ALD process is capable of producing a film of monolayer thickness. An ALD process is capable of producing layer after layer of monolayers. Instead of resulting in discrete increments of dielectric material, an ALD process is capable of creating a asymmetrical distribution of material. An ALD process is capable of creating a graded low tunnel barrier intergate insulator.

Endo does not disclose every aspect of the current subject matter. Furthermore, it is not obvious to modify Endo to achieve the subject matter recited in claim 1. In fact, due to the limitation of using a CVD process, Endo is believed to be incapable of achieving the subject matter recited in claim 1.

The Office Action states that "As for the limitation CVD as disclosed by the reference and the claimed multiple ALD, since the two processes both appear to result in an asymmetrical low tunnel barrier intergate insulator, the asymmetrical low tunnel barrier intergate insulator formed by multiple ALD is not patently distinguishable from the asymmetrical low tunnel barrier intergate insulator formed by CVD. As previously discussed, due to the amendment to claim 1, ALD and CVD do not result in the same asymmetrical low tunnel barrier intergate insulator. The CVD process in Endo results in a step-wise asymmetrical low tunnel barrier intergate insulator. The ALD process recited in claim 1 results in a graded asymmetrical low tunnel barrier intergate insulator.

The Office Action further states, "In addition, according to another doctrine, a process limitation, such as ALD, is considered a non-limitation in a product claim, if, as, or since the process does not result in a difference in structure..." Due to the amendment to claim 1, this doctrine no longer applies, as the process limitation certainly results in a difference in structure.

Applicant contends that in light of the amendment to claim 1, the burden of proof for an obviousness rejection under section 103 has not been satisfied. Furthermore, in light of the

amendment to claim 1, the burden of proof for an anticipation rejection under section 102 has not been satisfied. The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a non-volatile memory cell having all exclusive limitations as recited in claim 1. Therefore, Applicant respectfully requests that the Examiner withdraw his rejection to claim 1.

Dependent claims 2-9 are believed to be allowable for at least substantially similar reasons as those stated above with regard to parent claim 1.

§103 Rejection of the Claims

Claims 10, 11, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo in view of Orlowski et al. (U.S. 6,433,382). Withdrawal of the rejection is respectfully requested.

The Office Action bases the 103(a) rejection of claim 10 on the same basis as is detailed above for claim 1. Applicant respectfully traverses. The Office Action states the Endo discloses an asymmetrical low tunnel barrier intergate insulator with a small number of compositional ranges. However, claim 10 recites more limitations on the asymmetrical low tunnel barrier intergate insulator than a small number of compositional ranges. Claim 10 further recites: "a graded asymmetrical low tunnel barrier intergate insulator, formed by atomic layer deposition (ALD) having a number of small compositional ranges such that *gradients can be formed* which produce different barrier heights at an interface with the floating gate and control gate."

As previously discussed, Endo fails to teach a gradient in the intergate insulator. To create an intergate insulator, Endo uses CVD. CVD is believed incapable of producing a film at a thickness as small as a monolayer. As a result, Endo is incapable of producing an asymmetrical low tunnel barrier intergate insulator with a small number of compositional ranges such that gradients can be formed as recited in claim 10. Gradients cannot be formed using a CVD process. Gradients can be formed, however, using ALD process.

Because Endo fails to disclose an asymmetrical low tunnel barrier intergate insulator with a small number of compositional ranges such that gradients can be formed, the burden of proof necessary for a rejection based on obviousness has not been satisfied. The cited art, whether

taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious all exclusive limitations as recited in claim 1. As a result, Applicant respectfully requests that rejection of claim 10 is withdrawn.

Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo as applied to claim 1 above, and further in view of Eguchi et al. (U.S. 5,618,761). Withdrawal of the rejection is respectfully requested. Claims 5 and 6 depend from claim 1 and are allowable therewith over the applied references.

The Office Action states that "The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above including the asymmetrical low tunnel barrier intergate insulator." However, Endo discloses a step-wise configuration of the intergate insulator. Endo discloses only a step-wise configuration because Endo uses a CVD (deposition) process to form the low tunnel barrier intergate insulator. A CVD process is believed incapable of forming what is commonly known in the art as a monolayer. A monolayer is a film of material produced with a thickness of one atom. Because a CVD process is incapable of producing films with a thickness as small as a monolayer, it follows that a CVD process is also incapable of producing a graded low tunnel barrier intergate insulator. A CVD process is only capable of producing a larger thickness. Therefore, a CVD process is only capable of producing layers of low tunnel barrier intergate insulator in discrete increments, or "stepwise".

On the other hand, an ALD process is capable of producing a film of monolayer thickness. An ALD process is capable of producing layer after layer of monolayers. Instead of resulting in discrete increments of dielectric material, an ALD process is capable of creating a graded asymmetrical distribution of material. An ALD process is capable of creating a graded low tunnel barrier intergate insulator.

Not only does Endo not disclose a graded low tunnel barrier intergate insulator, Endo is believed to be incapable of doing so. Furthermore, it is not obvious to modify Endo to achieve the subject matter recited in claim 1. In fact, due to the limitation of using a CVD process, Endo is entirely incapable of achieving the subject matter recited in claim 1.

The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a non-volatile memory cell having all exclusive limitations as recited in claim 5 or claim 6. Therefore, Applicant respectfully requests that the Examiner withdraw his rejection to claims 5 and 6.

Claims 7-8, 12-13, and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo. These claims are believed allowable with their parent claims for at least the reasons stated above.

Claim 23 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo as applied to claim 18, and further in view of Orlowski et al. Claim 23 is believed to be allowable for at least substantially similar reasons as those stated above with regard to claims 10 and 18. Therefore, Applicant respectfully requests that the Examiner withdraw his rejection to claim 23.

Claims 2, 20-22, and 85-86 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Endo in view of Shinkawata et al. (U.S. 2002/0008324-A1). These claims are believed allowable with their parent claims for at least the reasons stated above.

Allowable Subject Matter

Claims 16-17, 19, and 87-95 were allowed.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 3 March '06

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3 day of March, 2006.

LISA ROSOWSKE

Name

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